PTO
10/038,9
01/02/

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10038209	01/02/2002	716	6	2825	Thompson

**APPLICANTS: Rich Marvin; Misra Ashutosh;

**CONTINUING DATA VERIFIED:

None

** FOREIGN APPLICATIONS VERIFIED:

None

PG-PUB | DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no	POU920010165US1
Verified and Acknowledged Examiner's Initials		

TITLE : Delay correlation analysis and representation for vita compliant VHDL models

U.S.DEPT. OF COMM./PAT & TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE	Application Examiner

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